Ka-Band Monolithic Low-Noise Amplifier Using Direct Ion-Implanted GaAs MESFET's

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***Abstract*—Ka-band monolithic low-noise amplifiers using low cost direct ion-implanted GaAs MESFET's with 0.25 μm "*T*"-gates have been developed for use at 27 to 34 GHz. The five stage MMIC amplifier is designed based on 50% Idss self-biasing using a single power supply. These amplifiers achieved 2–3 dB noise figure with 30 dB associated gain at 33 GHz. These results, using low cost ion implantation techniques, rival the best GaAs p-HEMT MMIC results to date.**

I. Introduction

ION implantation of the active device channel to fabricate MESFET's has long been recognized for its advantages in microwave MMIC fabrication. The ability to selectively implant planar devices combined with excellent uniformity, high throughput, and low cost makes ion implantation the most attractive method for large scale production. High volume applications such as smart munitions, intelligent vehicle highway system, and phased array antennas require cost-effective MMIC chips.

The first 60 GHz amplifier was reported in 1984 [1] using 0.3 μm gate length ion-implanted GaAs MESFET's. These MESFET's achieved a fairly impressive noise figure of 2.8 dB with an associated gain of 8.3 dB at 30 GHz. However, ion-implanted GaAs MESFET's at this time did not demonstrate an acceptable noise figure vis-á-vis GaAs HEMT's [2] to be useful in low-noise millimeter-wave IC applications. Then from 1989–1993, several groups [3]–[6] have demonstrated noise figure results for direct ion-implanted GaAs MESFET's which are comparable to GaAs p-HEMT's. The 0.25 $\times$ 200 μm gate ion-implanted GaAs MESFET has achieved a noise figure as low as 1 dB with 10 dB associated gain at 18 GHz. These results demonstrate that microwave noise performance of GaAs MESFET's can be made comparable to GaAs p-HEMT's. In 1991, an excellent three-stage low-noise amplifier fabricated using 0.25-μm gate ion-implanted GaAs MESFET's achieved a 4.2-dB noise figure with a 15 dB associated gain at Ka band [7].

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In this work, we review the design, simulation and fabrication of a five stage Ka-band low-noise amplifier demonstrating state-of-the-art gain and noise performance using a manufacturable, low cost, direct ion-implanted 0.25-μm gate GaAs MESFET technology.

II. GaAs MESFET's and LNA Fabrication

The GaAs MESFET's are fabricated by direct silicon and beryllium ion implantation into 3-in. semi-insulating (100) LEC GaAs substrates to form the active channel. The channel was formed by three distinct implants. The channel implant with a penetration depth of 1500 Å was used to achieve a peak carrier concentration of 1 $\times$ 10^{18} cm^{-3}; a penetration of 600 Å to achieve a peak carrier concentration of 2 $\times 10^{18}$ cm^{-3}; and a p-type implant of 50 keV to improve pinch-off characteristics. The implant was activated at the University of Illinois using a capless anneal technique with an arsine overpressure at 850°C [8]. The average sheet resistance is 220 Ω/square and the percent standard deviation is 1.4% for a typical wafer lot. The MESFET circuits were fabricated on the pilot line at Raytheons Advanced Device Center, Andover, MA. The standard 0.25-μm "*T*" gate is fabricated using an e-beam direct write technique. The gate was recessed to a target I_{dss} current of 180 mA/mm. The drain to source spacing is 3 μm and the source is air-bridge connected. Resistors are formed both by ion implantation and tantalum nitride. The wafers are fully passivated by silicon nitride. The wafers were then thinned to 100 μm for a backside via process.

III. GaAs MESFET's Performance

The current-voltage characteristic of the parallel gate MESFET is well behaved. The peak transconductance for 0.25 μm $\times$ 300 μm (4 $\times$ 75 μm) gate GaAs MESFET's is 105 mS (350 mS/mm). The corresponding transconductance gm = 280 mS/mm at V_{ds} = 1.5 V, and I_{ds} = 90 mA/mm. The current gain $|H_{21}|$ of the devices are calculated from measured S-parameters, and the f_t is determined by extrapolation using a slope of −6 dB/octave to the unity gain point, with the typical f_t = 60 GHz. The typical measured noise figure is 1.0 dB and the associated gain is 8.5 dB for I_{ds} = 45 mA/mm at 18 GHz. The self-bias of the LNA design is set at 90 mA/mm, where the noise figure is around 1.1 dB and the associated gain is 10 dB at 18 GHz.

The equivalent circuit model and scaled models for 0.25 μm $\times$ 100 μm (4 $\times$ 25 μm), 200 μm (4 $\times$ 50 μm) and

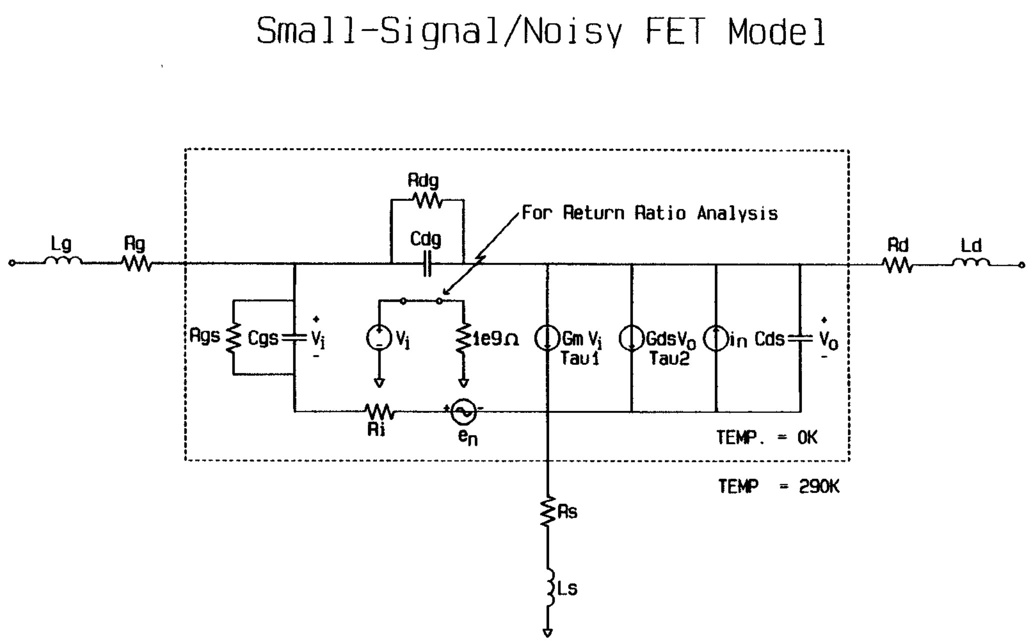

Fig. 1. Equivalent circuit model for 0.25-μm GaAs MESFET.

TABLE I
EQUIVALENT CIRCUIT SCALED MODEL VALUES FOR 0.25-μm GaAs MESFET AT 90 mA/mm

Parameter	units	Scaled Models		
Zg	mm	0.10	0.20	0.30
Vds	V	1.50	1.50	1.50
Ids	mA/mm	89.675	89.675	89.675
Vgs	V	−0.284	−0.284	−0.284
Ggs	mS	0.0005	0.0010	0.0015
Gdg	mS	0.0050	0.0100	0.0150
Rg	Ω	0.19	0.38	0.5
Rs	Ω	1.92	0.96	0.64
Rd	Ω	4.78	2.39	1.59
Ri	Ω	8.346	4.173	2.782
Gm	mS	28.59	57.17	85.76
Tau 1	pS	0.80	0.80	0.80
Gds	mS	3.025	6.050	9.075
Cgs	pF	0.0787	0.1574	0.2361
Cds	pF	0.0258	0.0561	0.0819
Cdg	pF	0.0268	0.0451	0.0635
Lg	pH	0.0	0.0	0.0
Ls	pH	3.64	2.76	2.32
Ld	pH	0.0	0.0	0.0
v, v*	$(nV)^2$/Hz	0.1374	0.0687	0.0458
i, i*	$(pA)^2$/Hz	510.6	1021.2	1531.8
Re v, i*	nV·pA/Hz	0.0139	0.0139	0.0139
Im v, i*	nV·pA/Hz	0.4028	0.4028	0.4028
f_t	GHz	57.81	57.81	57.81

300 μm (4 × 75 μm) GaAs MESFET are shown in Fig. 1 and Table I, respectively. This device model predicts noise measure, NM = 1.8 dB, and associated gain of 9 dB at 18 GHz, as well as NM = 3.2 dB and Ga = 5.5 dB at 33 GHz. The FET's for the device model was made 1.5 year ago, hence, the discrepancy between model and the current device using optimized implanted low noise schedule are expected. As a result, the LNA will be performed better than simulated results.

IV. Ka-Band Low-Noise Amplifier Design and Performance

The design goals for this Ka-band low-noise amplifier are: 1) >25-dB gain; 2) <3.5-dB noise figure; 3) >10-dBm output power at 33 GHz. The design employs a novel self-biased FET arrangement where Ids = 50%, Idss = 90 mA/mm, hence only a single power supply, V_{dd} = +3.0 V, is needed. The five-stage low-noise amplifier was composed of 0.1-mm-wide MESFET's for the first three stages, 0.2-mm-wide MESFET's for the fourth stage, and 0.3-mm-wide MESFET's for the fifth stage. The gate is grounded for the first three stages and has a 15 ohm resistor to ground in the last two stages. The voltage drop at each MESFET is 1.5 V. The design estimation of power consumption is 216 mW, where the nominal current of the whole circuit is 72 mA at a V_{dd} = 3 V. Using the EEsof-Libra simulator, this five-stage amplifier should achieve at least 23-dB gain and less than a 3.8 dB noise figure between 30 and 36 GHz operating frequency. The circuit simulation results show −15-dB input/output reflection coefficients over 30–36 GHz.

A SEM picture of the five stage Ka-Band low-noise amplifier is shown in Fig. 2. The chip size is 3.53 mm × 1.815 mm. The on-wafer millimeter wave performance for 10 samples of the LNA, biased with a single power supply of 3 V and Ids = 50% of Idss (84 mA) is shown in Fig. 3. The power consumption is 252 mW. The average on-wafer probe gain is 30 dB with a standard deviation of 0.6 dB, and on-wafer probe noise figure is between 2 and 3 dB over the frequency between 27 and 33 GHz. The input/output reflection coefficients are less than −10 dB at 33 GHz. The best fixtured noise performance is 2.3-dB noise figure with 31.4-dB associated gain at 33 GHz. These state-of-the-art results, using a single bias source represents about 15-dB higher gain and 1.5-dB lower noise figure than previous published three stage LNA results [7].

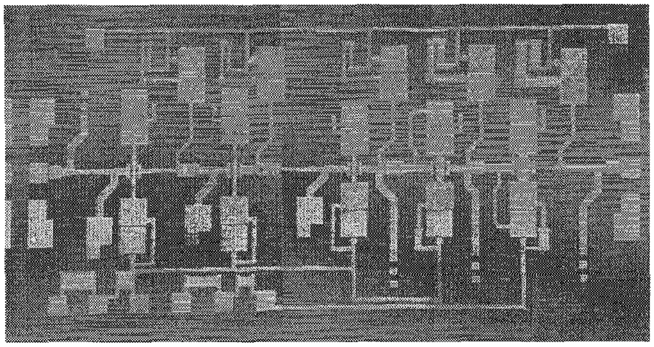

Fig. 2. SEM picture of five-stage Ka-Band low-noise amplifier.

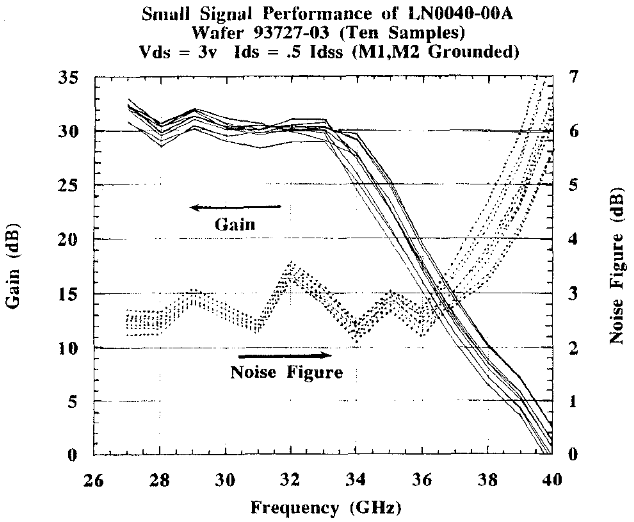

Fig. 3. Ten sample measurement of microwave gain and noise figure between 26–40 GHz.

Our results compare well with Ka-band LNA results achieved using GaAs p-HEMT technology which exhibits a 2.5-dB noise figure with 13-dB associated gain [9] and TRW 0.2-μm gate GaAs p-HEMT MMICS which demonstrates 3–4-dB noise figure with 10 dB gain at 35 GHz [10].

V. Conclusion

In this investigation, we demonstrate a specification compliant Ka-band LNA which serves to provide the first evidence that an ion-implanted low noise MESFET process can produce MMIC's devices which are equivalent or superior to the best pseudomorphic HEMT low-noise millimeter MMIC's. In addition, we have established state-of-the-art performance for a Ka-band low-noise amplifier. This work will enhanced the yield of monolithic millimeter-wave ICs using a simple low cost direct ion-implanted GaAs MESFET's technology. Further technology improvements of 0.1-μm "*T*" or "Γ" gates for direct ion-implanted GaAs MESFET's should enhance both gain and noise performance at Ka-band.

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